Digital Signals: News and Product Developments

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New AXIe Test Standard Proposed

Aeroflex Corporation, Agilent Technologies Inc., and Test Evolution Corporation today proposed a new modular test standard, AXIe (AdvancedTCA Extensions for Instrumentation and Test). AXIe is an open standard based on AdvancedTCA (ATCA) that creates a robust ecosystem of components, products and systems for general purpose instrumentation and semiconductor test. AXIe leverages existing standards from ATCA, PXI, LXI and IVI. These standards are used for automated test systems for both digital and analog products and systems. They provide defined operation and performance for digital control and communications, as well as analog interconnections between modules.

AXIe promises a number of key benefits for instrument designers that will improve their ability to meet the daunting test requirements from next-generation electronic products. AXIe offers higher performance per rack inch, greater scalability, easy integration with PXI, LXI and IVI, more modularity, more flexibility, and significant reduction of development and unit costs. AXIe is touted as an ideal complement to the LXI and PXI standards. It includes PCIe and LAN interfaces, so that AXIe instruments can act like virtual PXI or LXI instruments. A test system controller wouldn't be able to tell the difference, so an AXIe instrument can integrate seamlessly into a system, while yielding very high performance.

The ATCA PICMG 3.0 Standard—the foundation for the AXIe standard—is a proven open-system architecture with a large board size, which is ideal for high performance instrumentation. The result is rack space efficiency using either horizontal or vertical configurations. Users can integrate instrumentation from one slot to fourteen slots, one chassis to many chasses, or even use embedded PXI or PCI modules via adapters. ATCA is also ideal for high power applications with single rail power management and robust cooling. The AXIe standard is also structured to allow future extensions that can include Signal I/O, custom backplanes, and liquid cooling.

AXIe is a layered architecture. The foundation is ATCA (PICMG 3.0 and 3.4), which provides a large board size, LAN and PCIe as well as system management. The AXIe 1.0 builds upon this ATCA foundation for general purpose instrumentation adding core triggering capability, timing and a very high speed local bus. Extensions to AXIe 1.0 may be designed for specific application areas, such as semiconductor test (AXIe 1.1). For more information, see: www.axiestandard.org.

Test Tools and Methods for 10G EPON Chips

K-micro (Kawasaki Microelectronics America—www.k-micro.us), a maker of advanced ASICs, and Anritsu (www.us.anritsu.com) announce the development of the first test tool and methodology to analyze 10 Gbps Ethernet Passive Optical Network (EPON) chips. The successful test of K-micro's CTXL1 10G EPON SerDes chip using Anritsu's MP1800A Signal Quality Analyzer paves the way for 10G EPON systems to be shipped.

Precise measurements of K-micro's CTXL1 10G EPON SerDes chip demonstrate its innovative burst mode lock time of 20 ns. There are two major challenges to evaluate 10G EPON Optical Line Termination (OLT) burst mode SerDes:

- A Bit Error Rate Test (BERT) must examine only the delimiter and the payload, and calculate bit error rate. The sync pattern should not be taken into account.
- SerDes must keep the same latency for every burst. Or, the BERT must have the capability to allow latency difference between bursts.

The MP1800A's Pulse Pattern Generator (PPG) and Error Detector (ED) easily and accurately calculate the bit error rate, and CTXL1's Built In Self Test (BIST) function can successfully align the latency on every burst, so the BERT is not required to compensate for the variation of the latency between bursts. These two technologies make it possible to measure burst mode lock time at 10.3125 Gbps with BER of better than 1.0×10^{-12}.

500 MS/s Waveform Digitizer Uses PCI Express bus

AlazarTech, a manufacturer of high performance, low cost PC Based Instruments, has released the ATS9350®, a 12-bit, 500 MS/s, dual channel waveform digitizer based on the 8-lane PCI Express bus. One of the major differentiating features of the unit is its dual-port on-board acquisition memory buffer, which enables very fast, sustained data throughput to computer memory. Benchmarks run by the manufacturer show rates as high as 1.4 GigaBytes/s (not GigaBit/s) for sustained throughput over many hours.

The ATS9350 also has the ability to be externally clocked at frequencies as high as 500 MHz and as low as 1 MHz. This is very important for applications such as Optical Coherence Tomography (OCT) that require sampling to be synchronous with a non-uniform clock gener-

ated by a swept source laser. The latest generation of swept-source lasers output clocks can be as fast as 400 MHz and as slow as a few MHz.

Applications include OCT and other bio-medical imaging applications that require high dynamic range, external clocking and fast, sustained throughput for real-time signal processing; other scanning applications that involve acquisition of data with a rapidly occurring trigger (radar, ultrasonics, spectrometry, tomography, etc.); acquisition of data with a randomly occurring trigger (lightning test, acoustic emissions, etc.); and RF signal recording applications that require continuous streaming of data across the bus.

OEMs can integrate the ATS9350 PCI Express digitizers into their own systems using the Windows 7/Vista/XP compatible ATS-SDK Software Development Kit. This SDK includes sample programs written in C/C++ and Visual BASIC. A high performance LabVIEW® VI, called ATS-VI, is also available. A source code Linux driver, ATS-Linux, can also be made available to qualified customers, with a non-disclosure agreement. Information is available at: www.alazartech.com.

Common Mode Choke for USB 3.0

Designed specifically for USB 3.0 applications, Taiyo Yuden's new CM01S600 Common Mode Choke Coil delivers a 10 GHz cut off frequency. A 25% higher cutoff frequency improvement compared to previous products is achieved through the CM01S600's use of an extremely precise wire-wound structure.

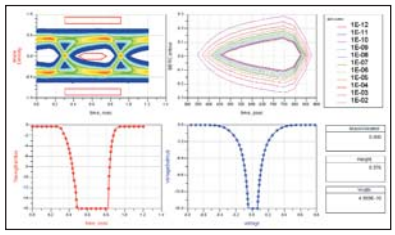
The higher cutoff frequency is necessary to support improvements in USB technology. USB is now available in a 3.0 version with speeds 10 times faster than the previous version. Because the new 3.0 USB uses high-speed differential signal transmission, practical applications of it requires that the resulting common mode noise be suppressed.

Taiyo Yuden's new CM01S600 is compact, measuring only 1.2 × 1.0 mm, with a maximum height of 0.9 mm. This common mode choke coil is currently being produced in volume quantities, The price is $0.20/unit. Information is available at: www.t-yuden.com.

Channel Simulator Option for ADS2009

Agilent Technologies Inc. has introduced a new statistical mode for its signal integrity Channel Simulator. The mode, offered as part of Agilent's Advanced Design System (ADS) 2009 Update 1, is well suited for design and verification of high-speed, chip-to-chip data links found in most consumer and enterprise digital products produced today—from laptop computers and data center servers, to telecommunication switching centers and Internet routers. By accelerating simulation, the new Channel Simulator mode allows manufacturers of such products to more quickly explore and arrive at an optimal design.

At today's multigigabit-per-second rates, high-frequency phenomena like impedance mismatch, reflections, crosstalk, skin effect and dielectric loss come into play. Agilent's Channel Simulator allows designers to perform simulations using circuit-level models that can be verified against measured data and EM simulation of the layout artwork.



In order to select the optimum set of characteristics for a transmitter, channel and receiver, signal integrity engineers need to determine ultralow bit-error-rate (BER) contours for thousands of points in the design space. Traditional techniques used to accomplish this task consume a prohibitively long simulation time.

Other signal integrity enhancements featured in ADS 2009 Update 1 include a BER contour and bathtub display; equalizer support with automatic tap optimization; an eye mask utility with automatic violation checking; the ability to check cross-talk with aggressors at different data rates; a memory bus compliance tool for the DDR3 standard; emitter-coupled logic models that comply with the IBIS standard; and a time-domain reflectometry tool. Information is available at: www.agilent.com/find/signal-integrity.

Multi-Frequency Clock Generator

Silicon Laboratories Inc. has expanded its Any-Rate Clock Generator family with the Si5355/56. The Si535x devices are made to order, 8-output CMOS clock generators capable of synthesizing four unique, non-integer related frequencies from 1–200 MHz. The Si535x clock generators provide guaranteed 0 ppm frequency synthesis error for any combination of frequencies, enabling the replacement of multiple clock ICs and crystal oscillators with a single device. Through a flexible web configuration utility called ClockBuilder™, factory-customized pin-controlled Si5355 devices are available in less than two weeks, enabling faster time to market while reducing the bill of materials in cost-sensitive networking, data communication, telecom access, computing and general purpose applications.

Modern hardware designs often require a diverse combination of non-integer related reference frequencies for processors, memory, and peripheral interfaces (e.g., Ethernet, PCI Express, USB, wireless LAN, IEEE1394, etc.). Traditionally, custom clocks have not been available for the broad market due to the need to generate

custom IC mask sets.

The Si5355 leverages a single PLL architecture and Silicon Labs' proven MultiSynth fractional divider technology to provide greater frequency flexibility and lower jitter than 3 PLL or 4 PLL clock generators. Since the Si5355 can synthesize all frequencies with 0 ppm error, it can replace multiple clock ICs and crystal oscillators with a single IC. The Si5355 has consistently low jitter (50 ps pk-pk period jitter) regardless of frequency configuration.

To further simplify design, the Si5355 can generate any combination of output frequencies from a standard, low cost 25 or 27 MHz crystal. If the device frequency plan changes, the same crystal can be reused, eliminating the higher cost associated with custom frequency crystals required by some traditional solutions. Alternatively, the Si5355 supports a 5–200 MHz reference clock input for synchronous applications.

Pricing for the Si5355 is $3.00 in 10k quantities. The Si5356 is priced at $3.60 in 10k quantities. The ClockBuilder utility is available at www.silabs.com/ClockBuilder. The Si5355-EVB and Si5356-EVB evaluation boards are available now and are each priced at $125. More information is available at: www.silabs.com.

Spectrum Analyzers Include Digital Demodulation

Aeroflex today announced the 3280A Series spectrum analyzers with 30 MHz digital demodulator and generic vector demodulation as standard features with no price increase over its predecessor, the 3280 Series. Digital demodulation in the 3280A Series spectrum analyzers allows engineers to analyze the transmitter characteristics of wireless devices. The 3280A Series includes many optional measurement suites including WiMAX, WLAN, UMTS, CDMA2000, and GSM/EDGE.

The 3280A Series spectrum analyzers are accurate, flexible, and easy-to-use. By including a 30 MHz digital demodulator as standard, the 3280A Series provides more functionality for the price, offering frequency coverage from 3 Hz to 26.5 GHz, top RF and microwave specifications, exceptional connectivity, and many ease-of-use features. Delivery for the 3280A Series is three weeks upon receipt of order, pending option configuration. Pricing for the series depends upon selections of bandwidth and options and begins at $16,000. Information is available at: www.aeroflex.com.

20 Gpbs Clocked Comparators

Hittite Microwave Corporation has launched a new family of 20 Gbps Clocked Comparators that offer a unique combination of low propagation delay for low input overdrive while minimizing propagation dispersion and power dissipation. The HMC874LC3C, HMC875LC3C and the HMC876LC3C are ideal for digital receivers, clock and data signal restoration, pulse spectroscopy, high speed instrumentation, medical imaging & diagnostics, and industrial systems. The devices are SiGe monolithic, ultra fast Clocked Comparators that feature high speed latches with programmable hysteresis, and reduced swing PECL/CML/ECL output drivers, respectively. They achieve 25 Gbps operation with reduced output voltage swing while providing 120 ps clock to data output delay. Minimum pulse width is typically 60 ps, and random jitter (RJ) is specified at only 0.2 ps rms. Information is available at www.hittite.com.